

DATA ACQUISITION SYSTEM AND TRIGGER ELECTRONICS FOR CACTUS

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CACTUS is a ground-based Air Cherenkov Telescope located at the Solar 2 facility in California, and operated by UC, Davis. It uses an array of 168 heliostats and a camera with 80 photomultiplier tubes to detect Cherenkov radiation produced by air showers. CACTUS incorporates novel techniques of time projection imaging and pattern triggering, implemented in FPGAs, thus improving upon the first generation sampling ACTs. Here we describe the telescope and its readout and triggering electronics.

1. Solar Two Field and CACTUS Secondary Optics

CACTUS (Converted Atmospheric Cherenkov Telescope Using Solar2) is a ground-based air-shower detector located near Barstow, California [1,2]. The Solar Two site consists of about 1,800 heliostats (42m^2 mirrors) that can be individually steered in elevation and azimuth. Motion controls are performed by remote-controlled driver electronics located at the base of each heliostat. Communications with a central computer are performed over a doubly-redundant system using RS-232 lines. The cumulative tracking and pointing error for each individual heliostat is about 0.1 arc-degree. CACTUS utilizes 168 of these heliostats that fall within the field-of-view of a secondary mirror mounted 60 m above ground level on a tower. These 168 are spread over $\sim 20,000\text{ m}^2$, thus providing a 35% coverage with their mirror area. The spherical secondary mirror is a composite mirror made out of 13 hexagonal facets, each 1m across. With an aperture of $4.4\text{m} \times 2.6\text{m}$ and a radius of curvature of 6m, it further focuses the 3m spot-size from the heliostats down to entrance apertures ($\sim 10\text{ cm}$) of light-collecting parabolic Winston cones located at the focal plane of the camera. The camera consists of 80 photomultiplier tubes (PMTs) positioned according to the spot sizes of heliostats on the focal plane. The upper 35 PMTs are positioned to align with individual heliostats, while the lower 45 PMTs form a close-packed matrix which allows images from multiple heliostats to be captured in a single channel. We have exploited this feature by implementing a scheme in which we later (offline) sort out the signals from heliostats by measuring the relative delays in the times of arrival. In order to accomplish this, we have built high bandwidth electronics that can provide two-pulse separation at the level of $\sim 5\text{ns}$. This is described below.

2. Readout and Trigger Electronics

There are four main components in the CACTUS data acquisition system shown in Figure 1: a) front-end amplifiers and discriminators, b) trigger system, c) time to digital converters (TDCs) and readout system and d) anode current recording.

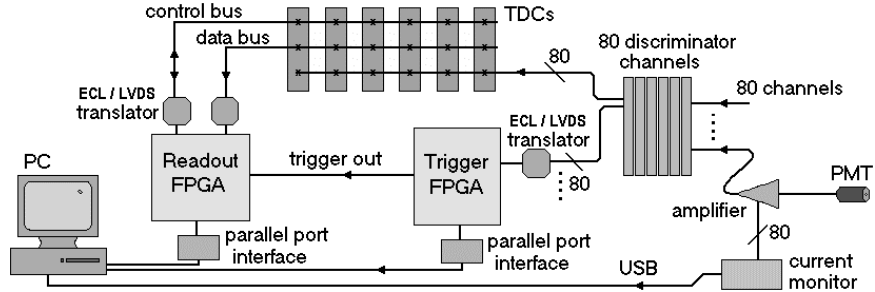


Figure 1: A box-diagram of the CACTUS amplification and readout system.

2.1 Analog Front-end

The front-end consists of inline (BNC-BNC) preamplifiers, mounted on the PMT bases, which drive 50 Ω co-axial cables to post-amplifiers located in a counting house. Both the preamps and the post-amps use monolithic broadband circuits (Mini-circuits ERA-3) [3] providing an overall voltage gain of $\sim 30\times$ and a bandwidth of ~ 1.6 GHz. The preamps are powered by a dc current carried on the same cable that is used for amplified pulses. A separate circuit senses this current and provides a voltage output that can be related to the anode current of the PMTs. The amplified signals are fed into CAMAC discriminators (LRS 4416) that provide dual outputs on ECL busses. The minimum pulse-width at the discriminator output is ~ 3.5 ns. Time-over-threshold measurements made above this minimum are directly proportional to pulse-heights. One set of ECL buses is connected to TDCs and the second one drives a trigger system.

2.2 Trigger System

The task of the trigger system, based around a Xilinx XCV1600 FPGA, is to determine the presence of an air-shower in a given 10 ns window. The decision time must be less than 1 μs because the storage depth in the TDCs is 2 μs . The ECL outputs from the discriminators are translated into LVDS levels before being fed into the FPGA. Figure 2 shows a schematic of the firmware loaded into the FPGA. It is divided into three main sections: a) delay lines, b) trigger logic and c) communications.

The pipelines are used dynamically in real time to delay the signals from each of the 80 input channels to compensate for flight path differences among photons arriving from different parts of the field. Figure 3 shows a schematic of a single channel pipeline. The building blocks consist of a flip-flop, a multiplexer and a decoder. These blocks are connected in a pipelined fashion such that an input signal gets introduced into the chain at a

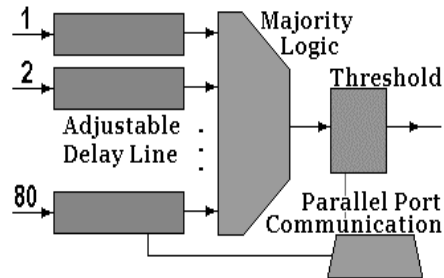


Figure 2: Schematic of the trigger system.

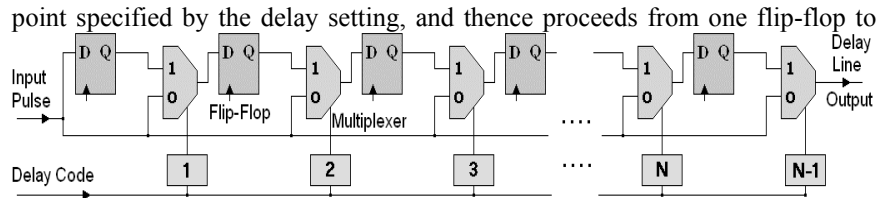


Figure 3: A schematic of the delay pipeline used in the trigger system.

the next with one step advanced every rising edge of the 100 MHz global clock. Once signals arrive at the end of the pipeline, each delayed by the specified amount, an air-shower is represented by pulses synchronized in time, within ~ 5 ns for gamma-ray showers and ~ 5 -20 ns for cosmic showers. Light from secondary heliostats clusters in distinct patterns in time and can be included in more complex triggering schemes to further improve efficiency.

The trigger logic is designed to detect timing patterns among the 80 channels. Various versions of the firmware can be downloaded into the FPGA. The simplest logic demands occupancy higher than some minimum number within a 10 ns window. Another version includes pulses from secondary heliostats and reconstructs the expected timing pattern for each channel. The “Majority Logic” module, which counts the number of channels with a hit in a 10 ns window, is pipelined in such a way that it uses only one logic cell per summing stage and is therefore capable of working at the required 100MHz clock. The summed value is truncated at six bits, thereby saving FPGA resources and making the electronics faster and more compact. This restricts the maximum allowed threshold to be 63. However, typical values used at CACTUS are in the 7-15 range. The “Threshold” module is a digital comparator which issues the final trigger when the sum value exceeds a user-specified threshold.

The third part of the design is responsible for communicating with the host computer via its parallel port. A software package running on the host computer provides updates to path delays in real time, based on the tracked source’s position in the sky. Delay data, in 8-bit format, are written to the data register of the parallel port and the FPGA loads them into an internal shift register that controls the delay pipelines. The coincidence level is also downloaded via the parallel port using its address register field.

2.3. Readout System

Data acquisition in CACTUS consists of recording time of arrival (TOA) and time over threshold (TOT) of all pulses that arrive up to $2 \mu\text{s}$ prior to the trigger time. This is accomplished by recording the rising and falling edges of discriminated signals in two different TDC channels, thus avoiding the minimum pulse-width constraint (8 ns) of the LRS 337 TDCs used in CACTUS. The TDCs register each edge independently with a 0.5 ns resolution. The TDCs are read out using a Xilinx XCV1000E FPGA as shown in Figure 4. The firmware used to program the FPGA is divided into three sections: a) TDC interface, b) 4-event buffer memory and c) data transfer, as described below.

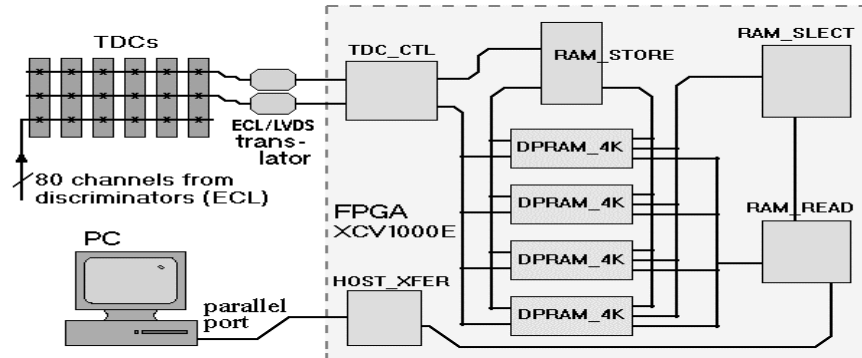


Figure 4: A schematic of the FPGA used in the TDC readout system.

The TDC_CTL module in figure 4 is an interface to the bank of TDCs via their front panel control bus. It implements a handshake protocol using 6 control lines: COM, WAK, REN are outputs and WST, BSY, PASS are inputs [4]. The TDCs are programmed in the “Common Stop” mode whereby they continuously acquire and store data in a 2 μ s buffer until a trigger is issued on the COM line. At this time the TDC stop recording and enter a readout mode. A handshake per word transfer (10 MHz) takes place between the TDC_CTL module and the TDCs. The BSY line stays high during valid data transfer and the PASS line is asserted at the end. The PASS line is daisy chained to the REN line of the next TDC, thus allowing for a sequential readout of several TDCs. The readout time for typical events at CACTUS is about 2-4 ms.

In order to minimize the system’s dead time, the data from the TDCs are stored in buffer memory modules, DPRAM_4K, which are dual port 4K RAMs. The RAM_STORE module controls buffer sequencing and data are stored in a cyclical fashion. The buffers themselves keep track of data record length and of their own status. In case an event is longer than 4K, it utilizes contiguous buffers until the entire event is stored or all the buffers are full. The read-back of the buffers when transferring data to the host computer is also done cyclically, such that the oldest data are read out first. The RAM_SELECT module gathers the MEMORY_STATE outputs from each of the four buffers and instructs the RAM_READ module on read out sequencing. In this scheme there is no deadtime due to transfer to host computer until the trigger rate gets high enough such that the average time between triggers is equal to the average data transfer time. CACTUS operates at trigger rates of \sim 20 Hz with less than 10% deadtime.

The HOST_XFER module implements an extended parallel port (EPP) protocol such that data can be transferred to the host computer’s parallel port, regardless of the state of the TDC readout module. There are six control lines involved in an EPP transfer: nDATASTB, nADDRSTB and nWRITE are generated by the host computer and nWAIT is asserted by the FPGA, while nRESET and nINTR are not used in this implementation. In addition, there is a bidirectional 8-bit bus that is used to transfer data and addresses. A C++

program, running on the host computer, continuously reads the address port for the presence of Hx0C which indicates that an event is ready to be read out from the FPGA buffer memory. The host reads a few header words followed by the event record which is transferred at the maximum allowed EPP rate of ~ 1 MHz.

2.4 Anode Current Readout

A voltage proportional to the PMT anode current is provided by the preamps and recorded using a commercial USB pod from National Instruments. The sampling rate can be varied in the 1-20 KHz range. The readout of these digitized voltages is asynchronous from the TDC readout and the data are correlated using time-stamps. The primary purpose of this data stream is for photometry which monitors the night sky background.

3. Results and Summary

Figure 5 shows a distribution of TOA from a sample of about 1,000 showers recorded by CACTUS. The lower curve is obtained by using only the primary heliostats (one per channel) while the upper curve includes pulses from secondary heliostats. The TOAs are with respect to a trigger time for that event and display a leading edge coherence of about 1 ns. The

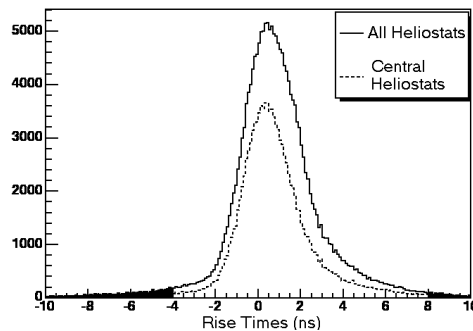


Figure 5: A histogram of recorded TOA.

trigger system provides a low threshold with an effective area of $\sim 10^4$ m² at 70 GeV rising to $\sim 6 \times 10^4$ m² at 500 GeV. In summary, CACTUS is operational and the electronics systems have met specifications. The telescope has measured the differential flux of the Crab Nebula [5] that is in agreement with the world dataset above 300 GeV and provides new data in the regime below 100 GeV.

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